

**ABSTRACT OF THE DISCLOSURE**

A data processing system 118 is provided that supports execution of both native instructions using a processor core and non-native instructions that are interpreted using either a hardware translator 122 or a software interpreter. Separate explicit return to non-native instructions and return to native instructions are provided for terminating subroutines whereby intercalling between native and non-native code may be achieved with reduced processing overhead. Veneer non-native subroutines may be used between native code and non-native main subroutines. The veneer non-native subroutines may be dynamically created within the stack memory region of the native mode system.

[Figure 19]